Customer No.: 31561
Application No.: 10/604,819
Docket No.: 11040-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original)A flash memory cell, comprising:

a substrate;

a stack gate structure formed on said substrate, said stack gate structure including a select gate dielectric layer, a select gate, and a gate cap layer, said select gate dielectric layer being formed between said substrate and said select gate, said gate cap layer being formed on said select gate;

a spacer formed along a sidewall of said select gate;

a control gate formed on one side of said stack gate structure and connected to said stack gate structure;

a floating gate formed between said control gate and said substrate and including a recess;

an inter-gate dielectric layer formed between said control gate and said floating gate;

a tunneling dielectric layer formed between said floating gate and said substrate; and

a drain region and a source region formed in said substrate, wherein said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively.

2. (original) The flash memory cell of claim 1, wherein a top surface of said floating gate layer is positioned between a top surface of said spacer and a top surface of said cap

layer.

3. (original) The flash memory cell of claim 1, wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide.

4. (original)A flash memory cell array, comprising:

a substrate;

a plurality of flash memory cell structures formed on said substrate, wherein each of said flash memory cell structures including

a stack gate structure formed on said substrate and including a select gate dielectric layer, a select gate, and a gate cap layer, wherein said select gate dielectric layer is formed between said substrate and said select gate, and said gate cap layer is formed on said select gate;

a spacer formed along a sidewall of said select gate;

a control gate formed on the one side of said stack gate structure and connected to said stack gate structure;

a floating gate formed between said control gate and said substrate;

an inter-gate dielectric layer formed between said control gate and said floating gate, wherein said control gate and said floating gate constitute a stack structure;

a tunneling dielectric layer formed between said floating gate and said substrate; and

a drain region and a source region formed in said substrate, said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively;

wherein said stack gate structure juxtaposes alternatively with said stack structure in said flash memory cell structures.

5. (original) The flash memory cell array of claim 4, wherein a top surface of said floating gate layer is positioned between a top surface of said spacer and a top surface of said gate cap layer.

6. (original)The flash memory cell array of claim 4, wherein said floating gate includes a recess, and said recess is substantially filled with said control gate.

7. (original) The flash memory cell array of claim 4, wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide.

8.-30. (cancelled).